MIPI CSI-2 Receiver IP Core

IP CORE FOR MIPI CSI-2 IMAGERS

AT A GLANCE

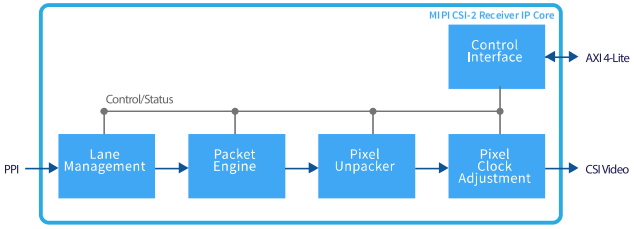
- MIPI CSI-2 receiver and decoding block
- Configurable number of MIPI Lanes
- Using Xilinx D-PHY IP
- Delivered with a reference design for fast development

In the machine vision industry, imagers using the MIPI CSI-2 interface get more and more popular. Many applications require the connection to an FPGA for advanced image pre-processing and further transfer to a host system. Sensor to Image's MIPI CSI-2 Receiver IP core provides a solution for decoding video streams from MIPI sensors in FPGAs. It requires a companion IP core implementing the MIPI D-PHY physical interface. The D-PHY receiver is connected to the CSI-2 receiver using the PHY-Protocol Interface (PPI). In order to shorten the development time, the MIPI CSI-2 Receiver IP core is delivered with a fully working reference design including Sensor to Image's MVDK and an IMX274 MIPI FMC module.

Main features

- FPGA technology independent
- PPI interface to connect to different D-PHY implementations
- Configurable to 1, 2 or 4 data lanes
- Any lane rate supported
- RAW8, RAW10, RAW12, RAW14, RAW16 standard MIPI data types supported
- Embedded data decoding supported
- Direct output of reordered byte stream without pixel unpacking supported
- AXI4-Lite slave control interface

The core is made of five main parts. The lane management together with the packet engine receive parallel byte lanes, extract control information, implement lane alignment and byte reordering, and finally provide aligned payload byte streams. The pixel unpacker extracts pixel data types out of these byte streams. The output pixel clock adjustment converts the pixel stream into the output clock domain. The control interface contains a set of control and status registers accessible by a CPU using the AXI4-Lite slave interface.



Delivery

The core is delivered with a complete reference design for S2I's MVDK with a Zynq Ultrascale+ FPGA, an IMX274 MIPI FMC module and a GigE Vision output. Since the physical interface is abstracted by the Xilinx D-PHY core, it is easy to port the design to other FPGA platforms like for example the 7 series Xilinx FPGAs.

Modules available

The MIPI CSI-2 Receiver IP Core is delivered as encrypted VHDL. It is optionally available as VHDL source code. It is compatible with Xilinx Artix7, Kintex7, Zynq7 and Ultrascale+ FPGAs.

The MIPI CSI-2 Receiver IP Software library is delivered as an object file. It is optionally available as C source code.

MVDK with MIPI CSI-2 Receiver interface board

RESOURCE USAGE

MODULE	ARTIX7 KINTEX7 ZYNQ7	ZYNQ ULTRASCALE+
Xilinx MIPI D-PHY 4 lanes		
External signal level conversion needed (for example Meticom chipset)	Yes	No
Registers	840	1188
Lookup Tables	2157	2261
BlockRAMs	0	0
MIPI CSI-2 Receiver IP Core configured for 4 lanes, 8-bit pixels		
Registers	793	793
Lookup Tables	286	285
BlockRAM	1	1